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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/802,799	03/18/2004	Takeshi Watanabe	250630US2S	5098

22850 7590 03/23/2005

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EXAMINER	
NGUYEN, DANG T	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 03/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/802,799	WATANABE ET AL.	
	Examiner	Art Unit	
	Dang T. Nguyen	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-6,10,12-15 and 18* is/are rejected.

7)☒ Claim(s) *2,7-9,11 and 16-17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 March 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/18/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *Search history*.

DETAILED ACTION

1. This action is responsive to the following communications: the Application and the Information Disclosure Statement filed on March 18, 2004.

2. Claims 1 – 18 are pending in this case. Claims 1, 10, and 18 are independent claims.

Priority

3. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3 - 6, 10, 12 - 15 and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Redgrave, U.S. patent No. 5,287,301 – filed Nov. 25, 1991.

Regarding independent claim 1, Figure 3 of Redgrave discloses a semiconductor memory comprising:

a first and a second field effect transistors [T1 and T1A] having a first line as gates of the first and second field effect transistors being connected to a reference electrode supplied with reference potential (Col. 5 lines 6-8);

a third and a fourth field effect transistors [T3A and T3] having a second line as gates, one ends of current paths the third and fourth field effect transistors being connected to the reference electrode [GND];

a fifth field effect transistor [T2] having a first word line as a gate (the word line gate from [T2] to [12]), one end of a current path of fifth field effect transistor being connected to the other ends of the current paths of the first and second field effect transistors (one end of [T2] and other ends [T1 and T1A] connect at [T5]); and

a sixth field effect transistor [T4] having a second word line as a gate (the word line gate from [T4] to [12]), one end of a current path of the sixth field effect transistor being connected to the other ends of the current paths of the third and fourth field effect transistors (one end of [T4] and other ends [T3 and T3A] connect at [T6]).

Regarding dependent claim 4, Figure 3 of Redgrave discloses wherein each of the first, second, third and fourth transistors [T1, T1A, T3A, and T3] forms a drive transistor (Abstract, lines 4-5), and each of the fifth and sixth [T2 and T4] transistors forms a transfer gate transistor (Col. 1 lines 43-44).

Regarding dependent claim 5, Figure 3 of Redgrave discloses further comprising: seventh field effect transistor [T6] having the first line as a gate; and an eighth field effect transistor [T5] having the second line as a gate.

Regarding dependent claim 6, Figure 3 of Redgrave discloses wherein one ends of current paths the seventh [T6] and eighth field effect transistors [T5] are connected to power supply electrode supplied with a power supply voltage [Vdd].

Regarding independent claim 10, Figure 3 of Redgrave discloses a semiconductor memory comprising:

a first and a second field effect transistors [T1 and T1A] having a first line as gates, one ends of current paths of the first and second field effect transistors being connected to a first reference electrode supplied with reference potential [GRD] (Col. 5 lines 6-8);

a third and a fourth field effect transistors [T3A and T3] having a second line as gates, one ends of current paths of the third and fourth field effect transistors being connected to a second reference electrode supplied with the reference electrode [GRD];

a fifth field effect transistor [T2] having a first word line as a gate (the word line gate from [T2] to [12]), one end of a current path of the fifth field effect transistor being connected to the other ends the current paths of the first and second field effect transistors (one end of [T2] and other ends [T1 and T1A] connect at [T5]); and

a sixth field effect transistor [T4] having a second word line as a gate (the word line gate from [T4] to [12]), one end of a current path of the sixth field effect transistor being connected to the other ends of the current paths of the third and fourth field effect transistors (one end of [T4] and other ends [T3 and T3A] connect at [T6]),

wherein the first, second and fifth [T1, T1A, and T2] field effect transistors are arranged symmetrically to the third, fourth and sixth [T3A, T3, and T4] field effect transistors, respectively, with respect a central point between the fifth field effect transistor and the sixth field effect transistor (see Figure 3).

Regarding dependent claim 13, Figure 3 of Redgrave discloses wherein each of the first, second, third and fourth transistors [T1, T1A, T3A, and T3] forms a drive transistor (Abstract, lines 4-5), and each of the fifth and sixth [T2 and T4] transistors forms a transfer gate transistor (Col. 1 lines 43-44).

Regarding dependent claim 14, Figure 3 of Redgrave discloses further comprising: seventh field effect transistor [T6] having the first line as a gate; and an eighth field effect transistor [T5] having the second line as a gate.

Regarding dependent claim 15, Figure 3 of Redgrave discloses wherein one ends of current paths the seventh [T6] and eighth field effect transistors [T5] are connected to power supply electrode supplied with a power supply voltage [Vdd].

Regarding independent claim 18, Figure 3 of Redgrave discloses a semiconductor memory comprising: a group of drive transistors [T1, T1A, T3A, and T3] including a plurality of field effect transistors, each of which having a current path having one end connected to a reference electrode supplied [Vdd] with a reference potential [GRD]; and a group of transfer gate transistors [T2 and T4] including a plurality of field effect transistors, each of which having a word line as a gate (the word line gate from [T2] to [12]) and having a current path with one end (one end of T2 connect to the others end T1 and T1A @ note 3 and 1 or at T5) connected to the other ends of the current paths of two of the field effect transistors included in the drive transistor group [T1 and T1A], the number of the field effect transistors of the transfer gate transistor group [T2 and T4] being smaller than the number of the field effect transistors included in the drive transistor group [T1, T1A, T3A, and T3].

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Redgrave, U.S. patent No. 5,287,301 – filed Nov. 25, 1991 in view of Applicant Admitted Prior Art (AAPA).

Regarding dependent claims 3 and 12, Redgrave as applied to claims 1 and 10 above disclosed every aspect of applicant's claimed invention except for wherein each of the first, second, third, fourth, fifth and sixth transistors includes a fin typed field effect transistor

Fig. 1 of AAPA discloses a fin typed field effect transistor (page 1, line 25 – page 2, line 7).

Redgrave and AAPA are common subject matter for SRAM and cross-coupled pair of transistors. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporated a fin typed field effect transistor taught by AAPA into first, second, third, fourth, fifth, and sixth transistors of Redgrave, since AAPA taught the benefit by pointing out that a transistor of a fin typed field effect transistor having a three-dimensional structure receive attention (page 1, line 25 – page 2, line 1).

Allowable Subject Matter

6. Claims 2, 7 - 9, 11, and 16 - 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

With respect to claims 2 and 11, the primary reason for indication of allowable subject matter is that the prior art fails to teach or suggest "wherein the current paths of the first and second field effect transistors are connected in parallel between the one end of the current path the fifth field effect transistor, and the current paths of the third and fourth field effect transistors are connected in parallel between the one end of the current path of the sixth field effect transistor.

With respect to claims 7 and 16, the primary reason for indication of allowable subject matter is that the prior art fails to teach or suggest "wherein the other ends the current paths of the first and second field effect transistors are connected to the other end of the current path of the seventh field effect transistor, and the other ends of the current paths of the third and fourth field effect transistors are connected to the other end of the current path of the eighth field effect transistor".

With respect to claims 8 and 17, the primary reason for indication of allowable subject matter is that the prior art fails to teach or suggest "wherein the gates of the first, second and seventh field effect transistors are connected to the other ends of the current paths of the third and fourth field effect transistors, and the gates of the third,

fourth and eighth field effect transistors are connected to the other end of the current path of the seventh field effect transistor".

With respect to claim 9, the primary reason for indication of allowable subject matter is that the prior art fails to teach or suggest "wherein the first, second, fifth and seventh field effect transistors are symmetrical to the third, fourth, sixth and eighth field effect transistors, respectively, with respect to a certain point".

Prior art

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Keshavarzi et al.	Patent No. US 6,181,608 B1	Date of Patent: Jan. 30, 2001
Kitazawa	Patent No. US 4,709,352	Date of Patent: Nov. 24, 1987

Contact Information

8. Any inquiry concerning this communication from the examiner should be directed to Dang Nguyen, who can be reached by telephone at (571) 272-1955. Normal contact times are M-F, 8:00 AM - 4:30 PM.

Upon an unsuccessful attempt to contact the examiner, the examiner's supervisor, Richard Elms, may be reached at (571) 272-1869.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist, whose telephone number is (703) 305-3900. The faxed phone number for organization where this application or

proceeding is assigned is (703) 872-9306.

Information regarding the Status of an application may be obtained from the patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair- direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free) or EBC@uspto.gov.

Dang Nguyen 3/15/2005

VAN THU NGUYEN
PRIMARY EXAMINER